# 74LV573

## Octal D-type transparent latch; 3-state

Rev. 03 — 28 September 2007 Product data sheet

## 1. General description

The 74LV573 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC573 and 74HCT573.

The 74LV573 consists of eight D-type transparent latches, featuring separate D-type inputs for each latch and 3-state true outputs for bus-oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

When LE is HIGH, data at the Dn inputs enters the latches. In this condition, the latches are transparent, that is, a latch output will change each time its corresponding D-input changes. When LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of LE.

When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The 74LV573 is functionally identical to the 74LV373, but has a different pin arrangement.

## 2. Features

- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC}$ = 2.7 V and $V_{CC}$ = 3.6 V
- Typical output ground bounce < 0.8 V at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C
- Typical HIGH-level output voltage ($V_{OH}$) undershoot: > 2 V at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Common 3-state output enable input
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LV573N | –40 °C to +125 °C | DIP20 | plastic dual in-line package; 20 leads (300 mil) | SOT146-1 |
| 74LV573D | –40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74LV573DB | –40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74LV573PW | –40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74LV573BQ | –40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

## 4. Functional diagram

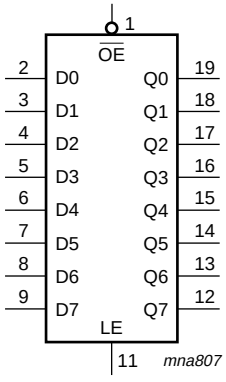



**Fig 1. Logic symbol**

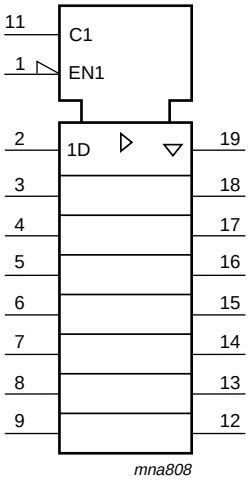



**Fig 2. IEC logic symbol**

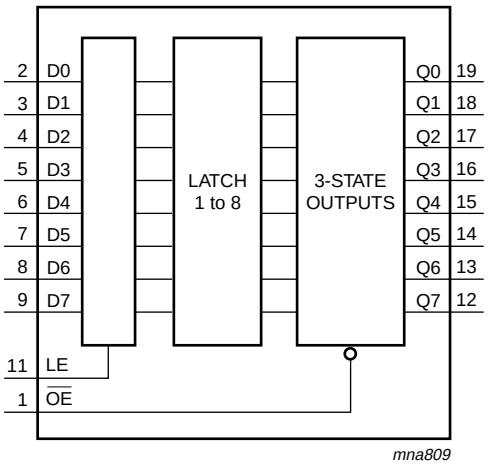



**Fig 3. Functional diagram**

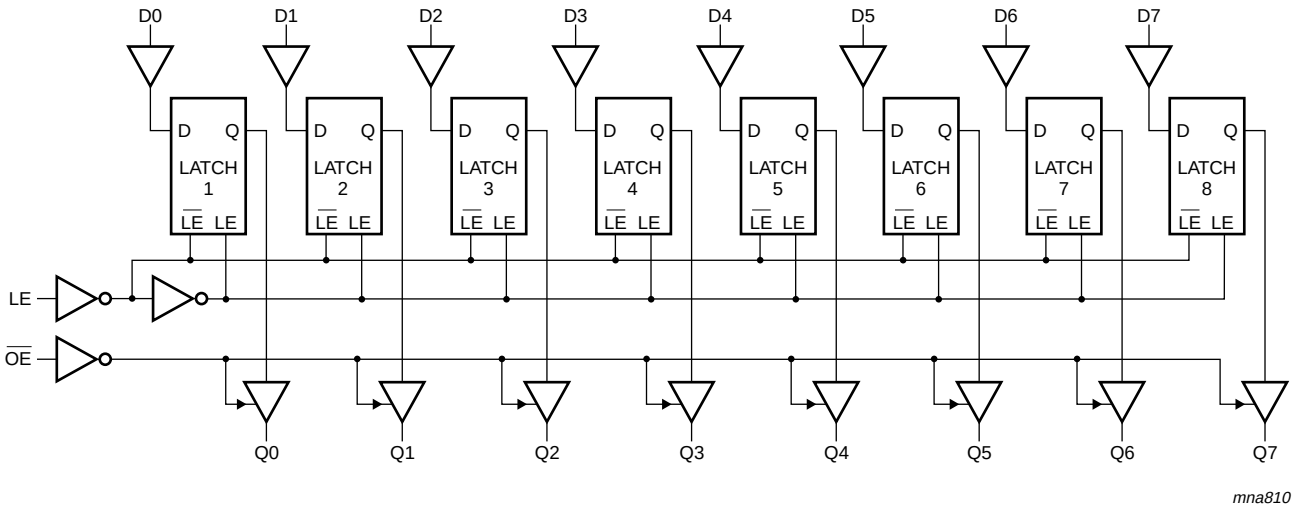



**Fig 4. Logic diagram**

# 5. Pinning information

## 5.1 Pinning

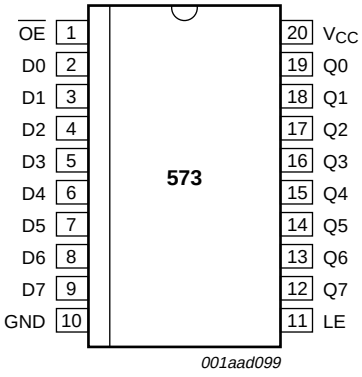
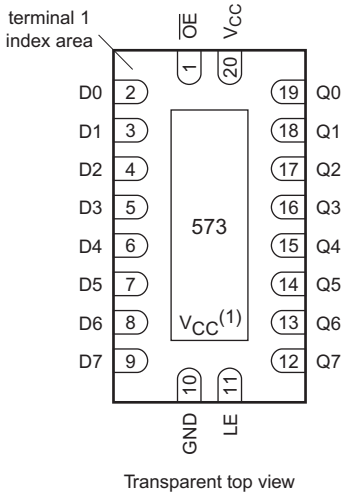



Fig 5. Pin configuration for SO20 and (T)SSOP20




(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 6. Pin configuration for DHVQFN20

## 5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| $\overline{OE}$ | 1 | output enable input (active LOW) |
| D[0:7] | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| GND | 10 | ground (0 V) |
| LE | 11 | latch enable input (active HIGH) |
| Q[0:7] | 19, 18, 17, 16, 15, 14, 13, 12 | data output |
| $V_{CC}$ | 20 | supply voltage |

## 6. Functional description

**Table 3. Functional table[1]**

| Operating modes | Input | | | Internal latch | Output |
|---|---|---|---|---|---|
| | $\overline{OE}$ | LE | Dn | | Qn |
| Enable and read register (transparent mode) | L | H | L | L | L |
| | L | H | H | H | H |
| Latch and read register | L | L | l | L | L |
| | L | L | h | H | H |
| Latch register and disable outputs | H | L | l | L | Z |
| | H | L | h | H | Z |

[1] H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high-impedance OFF-state

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | [1] | - | ±20 | mA |
| $I_{OK}$ | output clamping current | $V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] | - | ±50 | mA |
| $I_O$ | output current | $V_O = –0.5$ V to $(V_{CC} + 0.5$ V) | | - | ±35 | mA |
| $I_{CC}$ | supply current | | | - | 70 | mA |
| $I_{GND}$ | ground current | | | –70 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = –40$ °C to +125 °C | | | | |
| | DIP20 package | | [2] | - | 750 | mW |
| | SO20 package | | [3] | - | 500 | mW |
| | (T)SSOP20 package | | [4] | - | 500 | mW |
| | DHVQFN20 package | | [5] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[3] $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

[4] $P_{tot}$ derates linearly with 5.5 mW/K above 60 °C.

[5] $P_{tot}$ derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage[1] | | 1.0 | 3.3 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.0 V to 2.0 V | - | - | 500 | ns/V |
| | | $V_{CC}$ = 2.0 V to 2.7 V | - | - | 200 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 100 | ns/V |
| | | $V_{CC}$ = 3.6 V to 5.5 V | - | - | 50 | ns/V |

[1] The static characteristics are guaranteed from $V_{CC}$ = 1.2 V to $V_{CC}$ = 5.5 V, but LV devices are guaranteed to function down to $V_{CC}$ = 1.0 V (with input levels GND or $V_{CC}$).

## 9. Static characteristics

**Table 6. Static characteristics**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | 0.9 | - | - | 0.9 | - | V |
| | | $V_{CC}$ = 2.0 V | 1.4 | - | - | 1.4 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $0.7V_{CC}$ | - | - | $0.7V_{CC}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0.3 | - | 0.3 | V |
| | | $V_{CC}$ = 2.0 V | - | - | 0.6 | - | 0.6 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = –100 µA; $V_{CC}$ = 1.2 V | - | 1.2 | - | - | - | V |
| | | $I_O$ = –100 µA; $V_{CC}$ = 2.0 V | 1.8 | 2.0 | - | 1.8 | - | V |
| | | $I_O$ = –100 µA; $V_{CC}$ = 2.7 V | 2.5 | 2.7 | - | 2.5 | - | V |
| | | $I_O$ = –100 µA; $V_{CC}$ = 3.0 V | 2.8 | 3.0 | - | 2.8 | - | V |
| | | $I_O$ = –100 µA; $V_{CC}$ = 4.5 V | 4.3 | 4.5 | - | 4.3 | - | V |
| | | $I_O$ = –8 mA; $V_{CC}$ = 3.0 V | 2.4 | 2.82 | - | 2.2 | - | V |
| | | $I_O$ = –16 mA; $V_{CC}$ = 4.5 V | 3.6 | 4.2 | - | 3.5 | - | V |

**Table 6. Static characteristics** *...continued*

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.2 V | - | 0 | - | - | - | V |
| | | $I_O$ = 100 µA; $V_{CC}$ = 2.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 µA; $V_{CC}$ = 2.7 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 µA; $V_{CC}$ = 3.0 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 100 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.2 | - | 0.2 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 3.0 V | - | 0.20 | 0.40 | - | 0.50 | V |
| | | $I_O$ = 16 mA; $V_{CC}$ = 4.5 V | - | 0.35 | 0.55 | - | 0.65 | V |
| $I_I$ | input leakage current | $V_I = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | 1.0 | - | 1.0 | µA |
| $I_{OZ}$ | OFF-state output current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND; $V_{CC}$ = 5.5 V | - | - | 5 | - | 10 | µA |
| $I_{CC}$ | supply current | $V_I = V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 20 | - | 160 | µA |
| $\Delta I_{CC}$ | additional supply current | per input; $V_I = V_{CC}$ – 0.6 V; $V_{CC}$ = 2.7 V to 3.6 V | - | - | 500 | - | 850 | µA |
| $C_I$ | input capacitance | | - | 3.5 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V; For test circuit see Figure 11.*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | Dn to Qn; see Figure 7 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 75 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 26 | 39 | - | 49 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 19 | 29 | - | 36 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V; $C_L$ = 15 pF | [3] | - | 12 | - | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 14 | 23 | - | 29 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | - | 19 | - | 24 | ns |
| | | LE to Qn; see Figure 8 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 80 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 27 | 43 | - | 53 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 20 | 31 | - | 34 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V; $C_L$ = 15 pF | [3] | - | 13 | - | - | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 15 | 25 | - | 31 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | - | 21 | - | 26 | ns |

**Table 7. Dynamic characteristics** *...continued*

*GND = 0 V; For test circuit see Figure 11.*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{en}$ | enable time | $\overline{OE}$ to Qn; see Figure 9 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 70 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 24 | 37 | - | 48 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 18 | 28 | - | 35 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 13 | 22 | - | 28 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | - | 18 | - | 23 | ns |
| $t_{dis}$ | disable time | $\overline{OE}$ to Qn; see Figure 9 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 80 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | - | 29 | 39 | - | 48 | ns |
| | | $V_{CC}$ = 2.7 V | | - | 22 | 29 | - | 36 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | - | 17 | 24 | - | 29 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | - | 20 | - | 24 | ns |
| $t_W$ | pulse width | LE HIGH; see Figure 8 | | | | | | | |
| | | $V_{CC}$ = 2.0 V | | 34 | 9 | - | 41 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 25 | 6 | - | 30 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 20 | 5 | - | 24 | - | ns |
| $t_{su}$ | set-up time | nD to nCP; see Figure 10 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 25 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 17 | 9 | - | - | 20 | ns |
| | | $V_{CC}$ = 2.7 V | | 13 | 6 | - | - | 15 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 10 | 5 | - | - | 12 | ns |
| $t_h$ | hold time | Dn to LE; see Figure 10 | | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 5 | - | - | - | ns |
| | | $V_{CC}$ = 2.0 V | | 8 | 2 | - | 8 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 8 | 2 | - | 8 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [3] | 8 | 1 | - | 8 | - | ns |
| $C_{PD}$ | power dissipation capacitance | $C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ | [4] | - | 26 | - | - | - | pF |

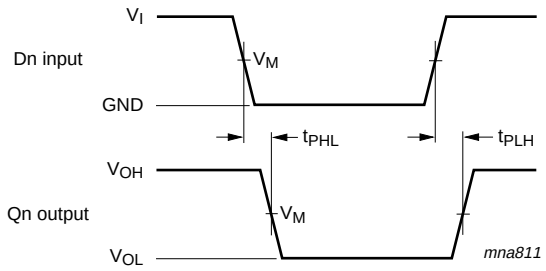
[1] All typical values are measured at $T_{amb}$ = 25 °C.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[3] Typical values are measured at nominal supply voltage ($V_{CC}$ = 3.3 V).

[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz
$C_L$ = output load capacitance in pF
$V_{CC}$ = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

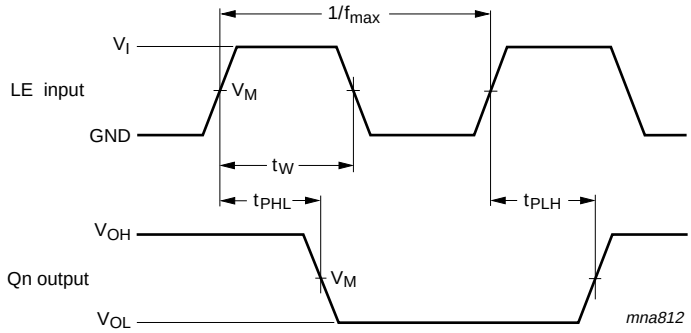
## 11. Waveforms




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

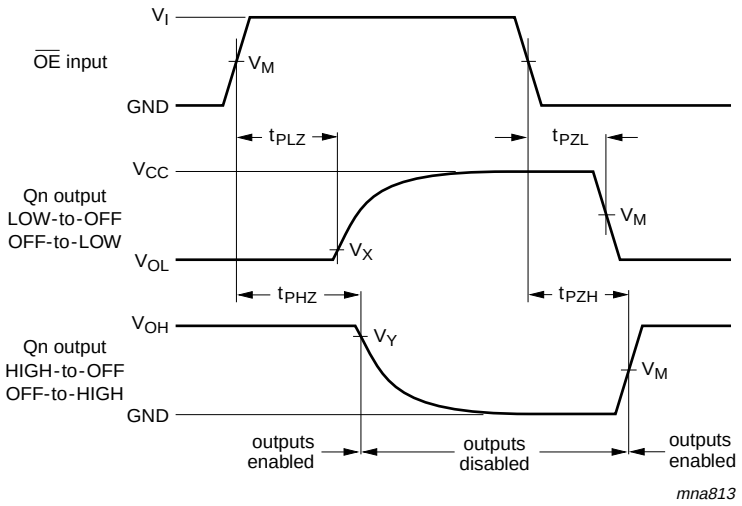
**Fig 7. Input (Dn) to output (Qn) propagation delays**




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

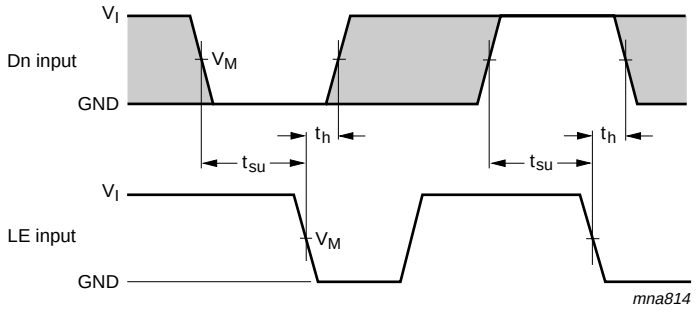
**Fig 8. Latch Enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays**




Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 9. Enable and disable times**



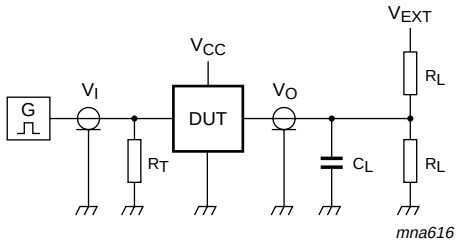

Measurement points are given in Table 8.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 10. Data set-up and hold times for the Dn input to the LE input**

**Table 8. Measurement points**

| Supply voltage | Input | Output | | |
|---|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| < 2.7 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.1V_{CC}$ | $V_{OH} - 0.1V_{CC}$ |
| 2.7 V to 3.6 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ – 0.3 V |
| ≥ 4.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.1V_{CC}$ | $V_{OH} - 0.1V_{CC}$ |




Test data is given in Table 9.

Definitions test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

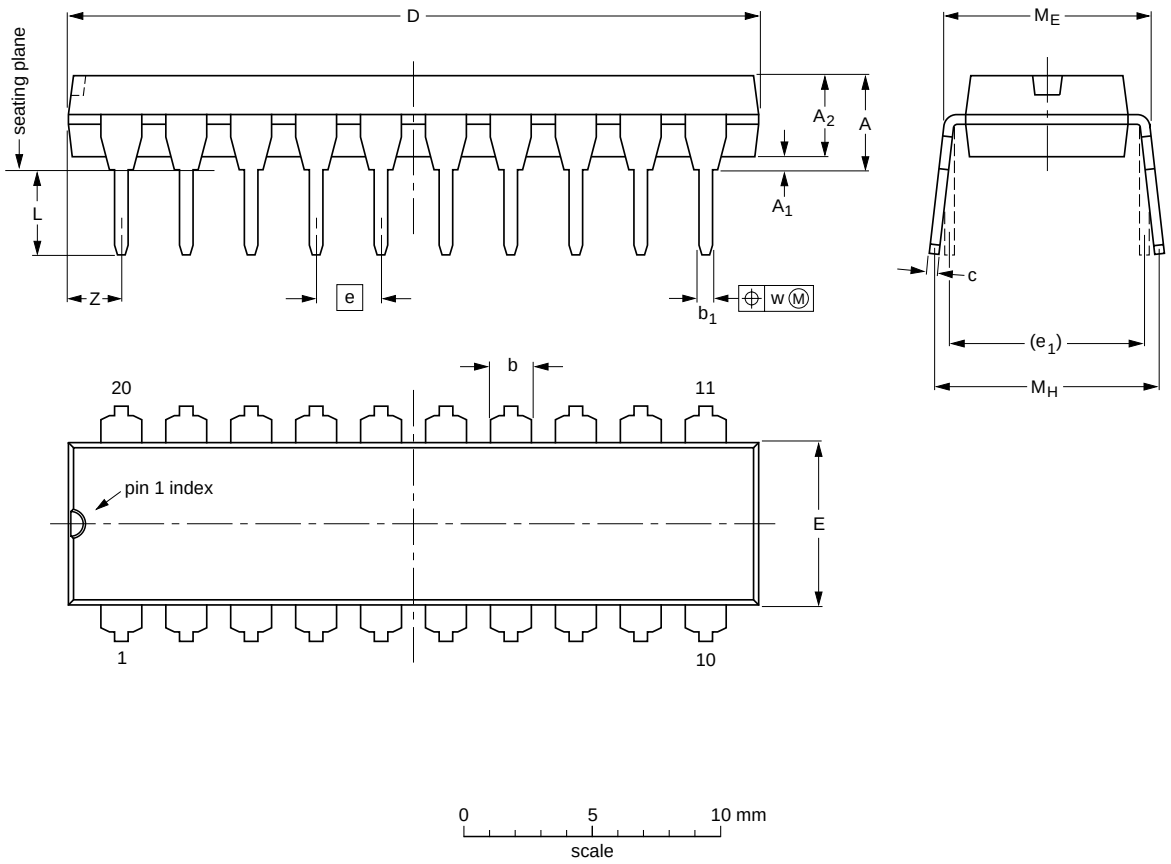
**Fig 11. Load circuit for switching times**

**Table 9: Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHL}$, $t_{PLH}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| < 2.7 V | $V_{CC}$ | ≤ *2.5 ns* | 50 pF | 1 kΩ | open | GND | $2V_{CC}$ |
| 2.7 V to 3.6 V | 2.7 V | ≤ *2.5 ns* | 15 pF, 50 pF | 1 kΩ | open | GND | $2V_{CC}$ |
| ≥ 4.5 V | $V_{CC}$ | ≤ *2.5 ns* | 50 pF | 1 kΩ | open | GND | $2V_{CC}$ |

## 12. Package outline

**DIP20: plastic dual in-line package; 20 leads (300 mil)** **SOT146-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 0.36<br>0.23 | 26.92<br>26.54 | 6.40<br>6.22 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 2 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.014<br>0.009 | 1.060<br>1.045 | 0.25<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.078 |

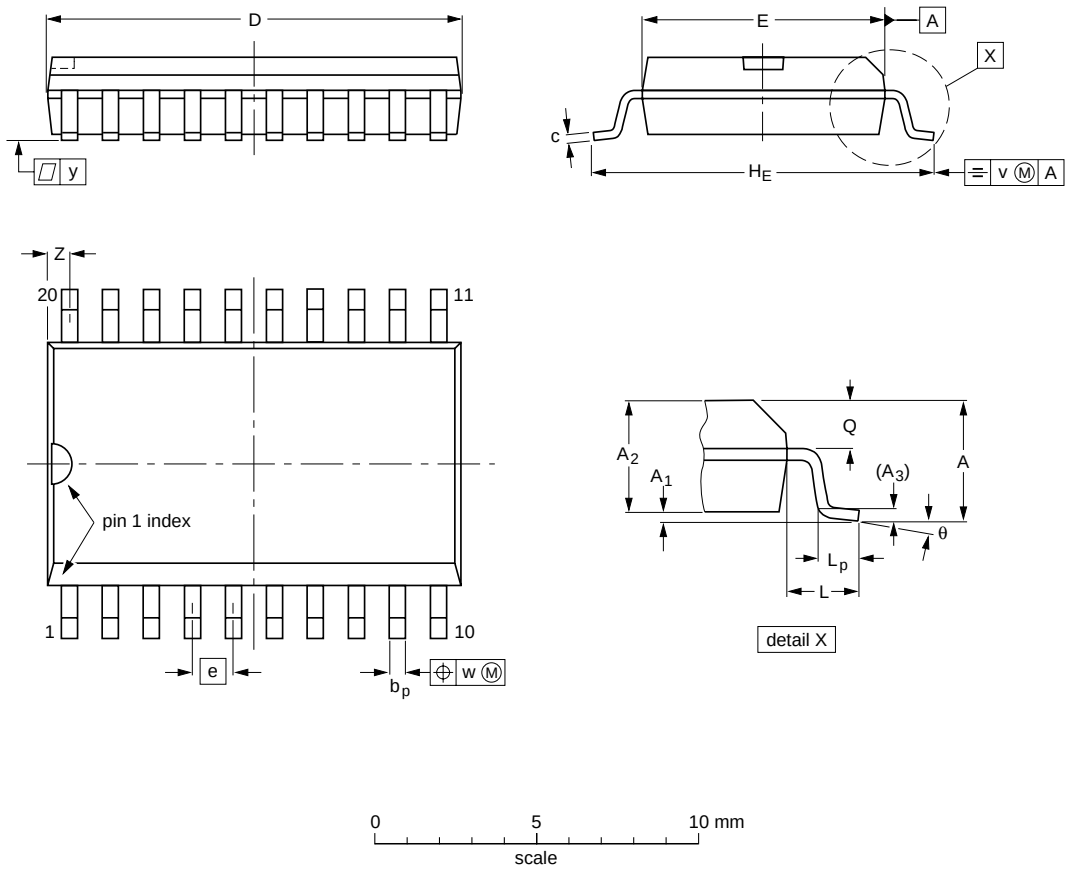
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT146-1 | | MS-001 | SC-603 | | | ~~99-12-27~~<br>03-02-13 |

**Fig 12. Package outline SOT146-1 (DIP20)**

**SO20: plastic small outline package; 20 leads; body width 7.5 mm** **SOT163-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 13.0<br>12.6 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.51<br>0.49 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

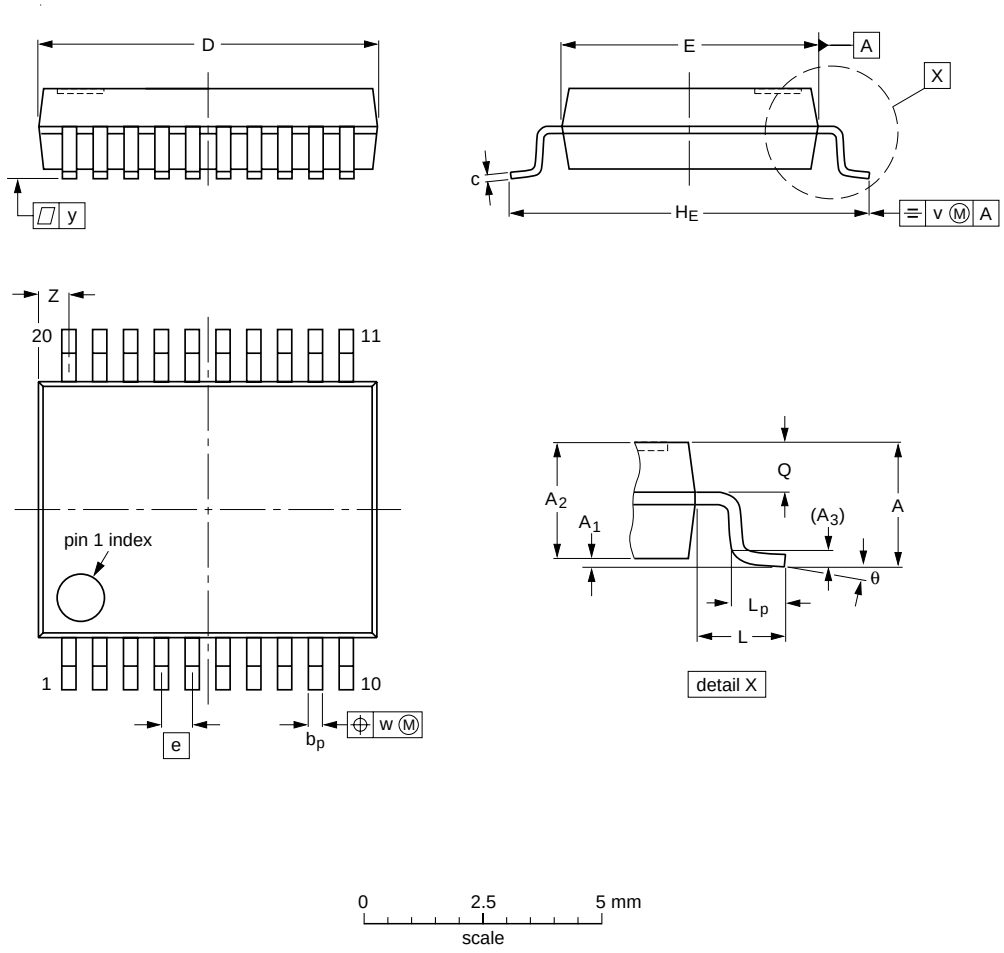
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT163-1 | 075E04 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 13. Package outline SOT163-1 (SO20)**

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm** **SOT339-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 7.4<br>7.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.9<br>0.5 | $8^o$<br>$0^o$ |

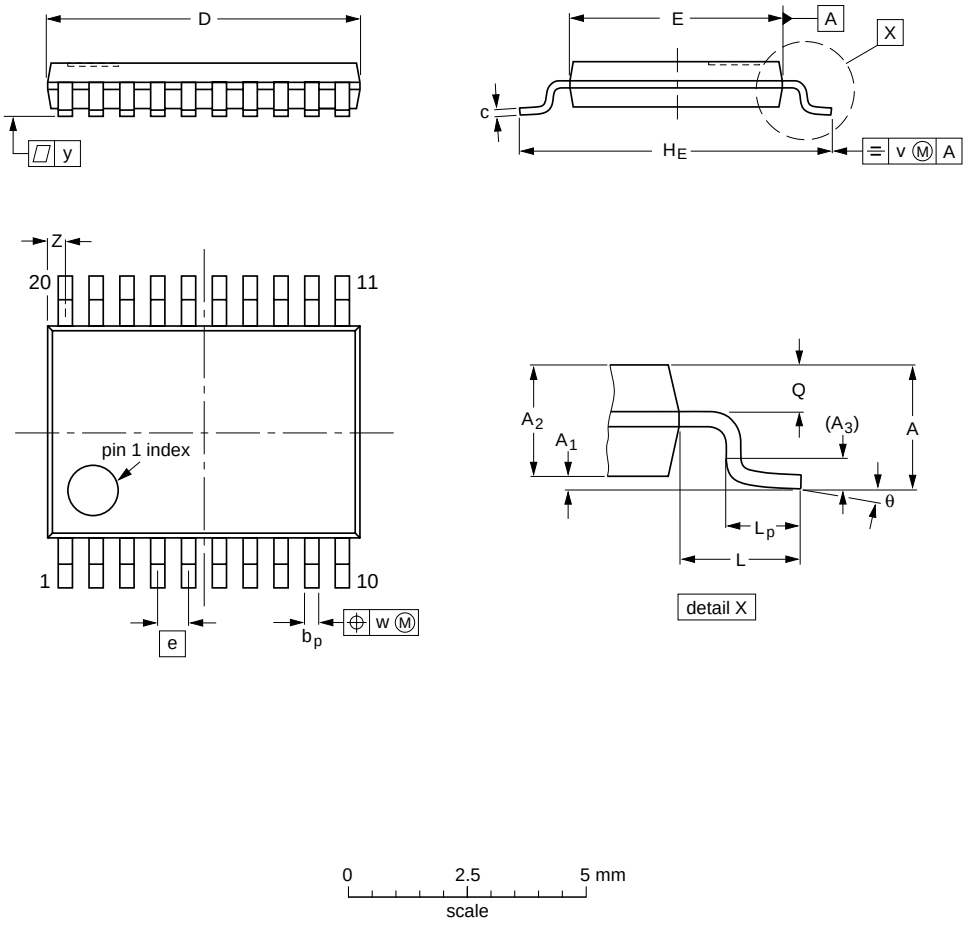
**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT339-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 14. Package outline SOT339-1 (SSOP20)**

**TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm** **SOT360-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 6.6<br>6.4 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | $8^o$<br>$0^o$ |

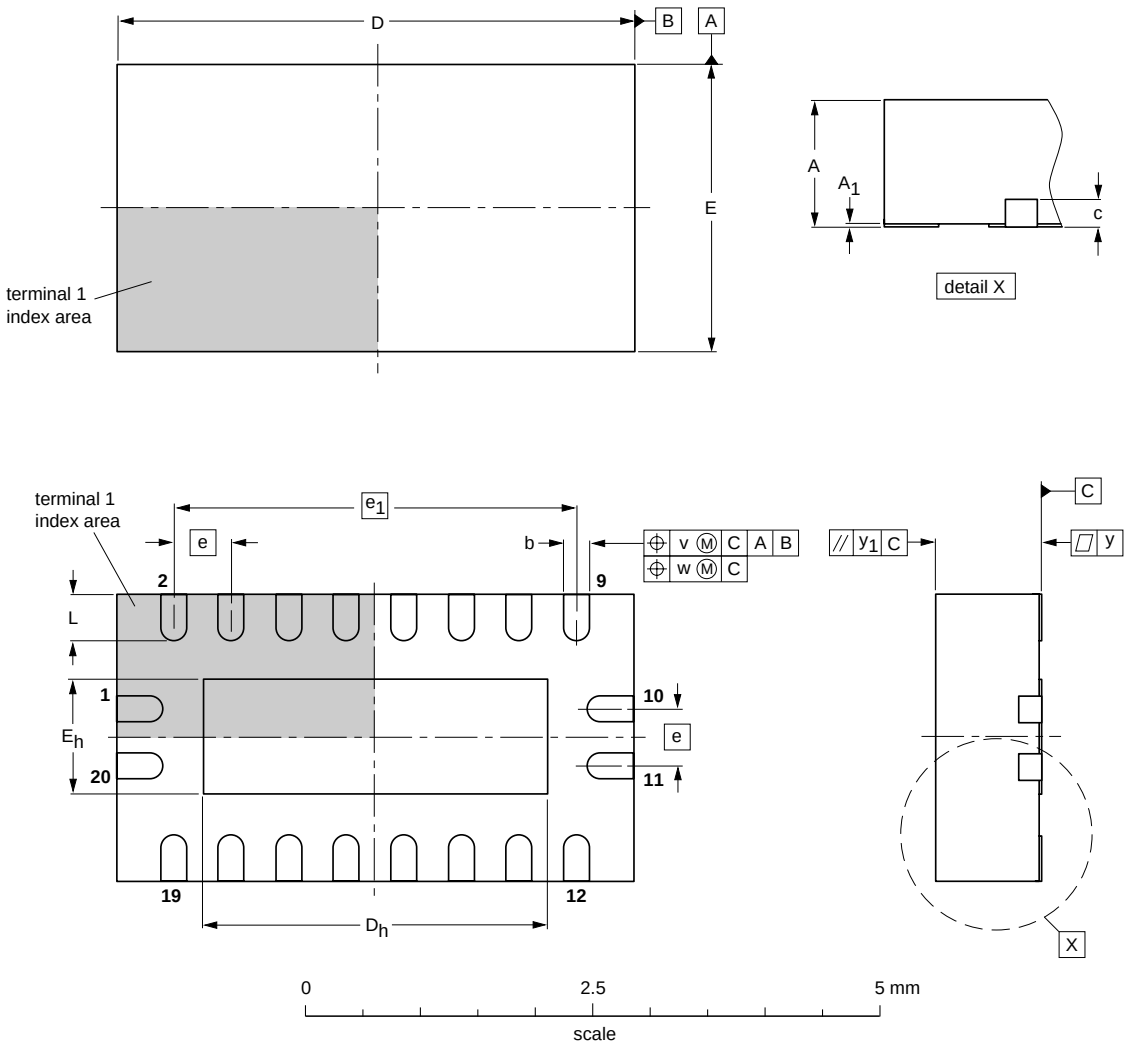
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT360-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 15. Package outline SOT360-1 (TSSOP20)**

**DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm** **SOT764-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 4.6<br>4.4 | 3.15<br>2.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 3.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT764-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 16. Package outline SOT764-1 (DHVQFN20)**

## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LV573_3 | 20070928 | Product data sheet | - | 74LV573_2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name when appropiate.<br>• Section 3: DHVQFN20 package added.<br>• Section 8: derating values added for DHVQFN20 package.<br>• Section 12: outline drawing added for DHVQFN20 package. | | | |
| 74LV573_2 | 19980610 | Product specification | - | 74LV573_1 |
| 74LV573_1 | 19970606 | Product specification | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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